

JC 926

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Class	Subclass
ISSUE CLASSIFICATION	

03/10/01

PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.

PATENT DATE

FA
SCANNED 03/10/01

APPLICATION NO. 09/823058	CONT/PRIOR F	CLASS 432	SUBCLASS 761	ART UNIT 3834	EXAMINER L. GENTILINI MILLS MORRIS
APPLICANTS Tatsuya Suzuki		156 345.31		1763	
TITLE Struct/transistor layer of semiconductor substrate and method of manufacturing semiconductor device					

PTO-2040
12/89

ISSUING CLASSIFICATION

TERMINAL DISCLAIMER	DRAWINGS				
	Sheets Drwg. 5	Figs. Drwg. 7	Print Fig. 3	Total Claims 1	Claims Checked O.O.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	KAPLA MOORE 4/14/03 (Assistant Examiner) (Date)			NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent No. _____					
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	(Primary Examiner) (Date)			ISSUE FEE	
	(Legal Instruments Examiner) (Date)			Amount Due	Date Paid
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